PCI-5105 Specifications

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Contents

PCI-5105 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All filter settings
- All impedance selections
- Sample clock set to 60 MS/s

Warranted specifications are valid under the following conditions unless otherwise noted.

- Temperature range of 0 °C to 45 °C
- The PCI-5105 module is warmed up for 15 minutes at ambient temperature
- Calibration cycle is maintained

- The PCI chassis fan speed is set to HIGH, the foam fan filters are removed if present, and all filler panels are installed. For more information about cooling, refer to the **Maintain Forced-Air Cooling Note to Users** available at ni.com/manuals.
- External calibration is performed at 23 °C ± 3 °C

Vertical

Analog Input

Number of channels	Eight (simultaneously sampled)
Input type	Referenced single-ended
Connectors	SMB

Impedance and Coupling

Input impedance	
50 Ω	50 Ω ±2%
1 MΩ	1 MΩ ±1% in parallel with a nominal capacitance of 50 pF
Input coupling	AC[1], DC

Voltage Levels

Full-scale (FS) input range	
50 Ω and 1 MΩ	0.05 V
	0.2 V

	1 V
	6 V
1 MΩ only	30 V

Maximum input overload

50 Ω	7 V_{rms} with |Peaks| ≤10 V
1 MΩ	|Peaks| ≤42 V

Accuracy

Resolution	12 bits

Input Impedance	Input Range (V_{pk-pk})	DC Accuracy, Warranted
50 Ω	All	±(1% × **Reading** + 0.25% of FS + 1.4 mV)
1 MΩ	0.05 V	±(1% × **Reading** + 0.25% of FS + 1.4 mV)
	0.2 V, 1 V, and 6 V	±(0.65% × **Reading** + 0.25% of FS + 1.4 mV)
	30 V	±(0.75% × **Reading** + 0.25% of FS + 1.4 mV)

Table 1. DC Accuracy[2]

DC drift	±(0.05% of **Reading** + 0.02% of FS + 20 µV) per °C

Input Impedance	Input Range (V_{pk-pk})	AC Amplitude Accuracy
50 Ω	All	±0.1 dB (±1.2%) of **Reading**
1 MΩ	0.05 V	±0.2 dB (±2.3%) of **Reading**
	0.2 V and 1 V	±0.13 dB (±1.5%) of **Reading**
	6 V and 30 V	±0.4 dB (±4.7%) of **Reading**

Table 2. AC Amplitude Accuracy[3]

Input Impedance	Input Range (V_{pk-pk})	Crosstalk
50 Ω	All	≤-80 dB at 1 MHz
1 MΩ	0.05 V	≤-75 dB at 1 MHz
	0.2 V, 1 V, 6 V, and 30 V	≤-80 dB at 1 MHz

Table 3. Crosstalk[4]

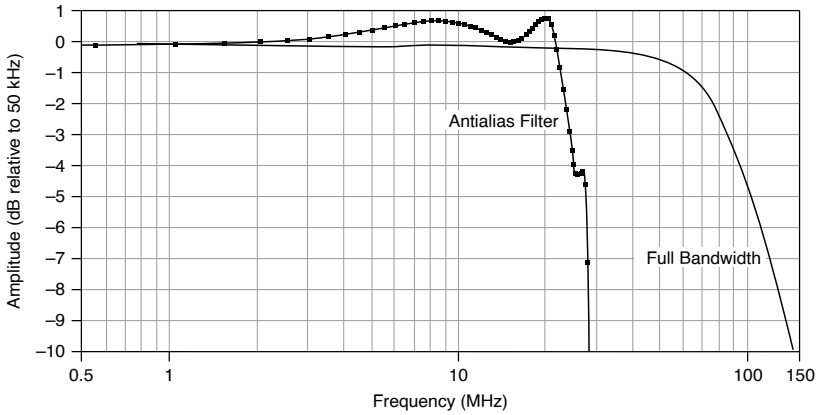
Bandwidth and Transient Response

Input Impedance	Input Range (V_{pk-pk})	Bandwidth
50 Ω	0.05 V	55 MHz
	0.2 V, 1 V, and 6 V	60 MHz
1 MΩ	0.05 V	35 MHz
	0.2 V, 1 V, 6 V, and 30 V	60 MHz

Table 4. Bandwidth (-3 dB)

Bandwidth-limiting filter	24 MHz anti-alias filter
AC-coupling cutoff (-3 dB)[5]	12 Hz

Figure 1. Frequency Response, 50 Ω, 1 V_{pk-pk} Input Range, Measured



Spectral Performance

> **Note** Due to high spectral noise content below 5 kHz caused by some computer chassis, spectral performance for the PCI-5105 is specified for 5 kHz and above on the indicated ranges. For more information on preventing ground loop noise, refer to the **PCI and PXI Ground Loop Noise** topic available at ni.com/manuals.

1 MΩ Spectral Performance[6]

Input Range (V_{pk-pk})	SFDR
0.2 V	70 dBc (≥5 kHz)
1 V and 6 V	65 dBc

Table 9. Spurious-Free Dynamic Range (SFDR)

Input Range (V_{pk-pk})	THD
0.05 V	-72 dBc
0.2 V	-75 dBc
1 V	-65 dBc
6 V	-68 dBc

Table 10. Total Harmonic Distortion (THD)

Input Range (V_{pk-pk})	SINAD
0.05 V	50 dB (≥5 kHz)
0.2 V	59 dB (≥5 kHz)
1 V	61 dB
6 V	59 dB

Table 11. Signal to Noise and Distortion (SINAD)

1 MΩ Noise

Input Range (V_{pk-pk})	Full Bandwidth	24 MHz Filter Enabled
0.05 V	0.18% of FS (90 µV) (≥5 kHz)	0.12% of FS (60 µV) (≥5 kHz)
0.2 V	0.060% of FS (120 µV) (≥5 kHz)	0.036% of FS (72 µV) (≥5 kHz)
1 V	0.03% of FS (300 µV)	0.03% of FS (300 µV)
6 V	0.055% of FS (3.3 mV)	0.036% of FS (2.16 mV)
30 V	0.03% of FS (9 mV)	0.03% of FS (9 mV)

Table 12. 1 MΩ RMS Noise[7]

50 Ω Spectral Performance

Input Range (V_{pk-pk})	SFDR
0.2 V	72 dBc (≥5 kHz)
1 V and 6 V	72 dBc

Table 9. Spurious-Free Dynamic Range (SFDR)[8]

Input Range (V_{pk-pk})	THD
All	-75 dBc

Table 10. Total Harmonic Distortion (THD)[8]

Input Range (V_{pk-pk})	SINAD
0.05 V	59 dB (≥5 kHz)
0.2 V to 6 V	62 dB

Table 11. Signal to Noise and Distortion (SINAD)[8]

Figure 2. PCI-5105 Dynamic Performance, 50 Ω, 1 V_{pk-pk}, with 24 MHz Filter Enabled, Measured

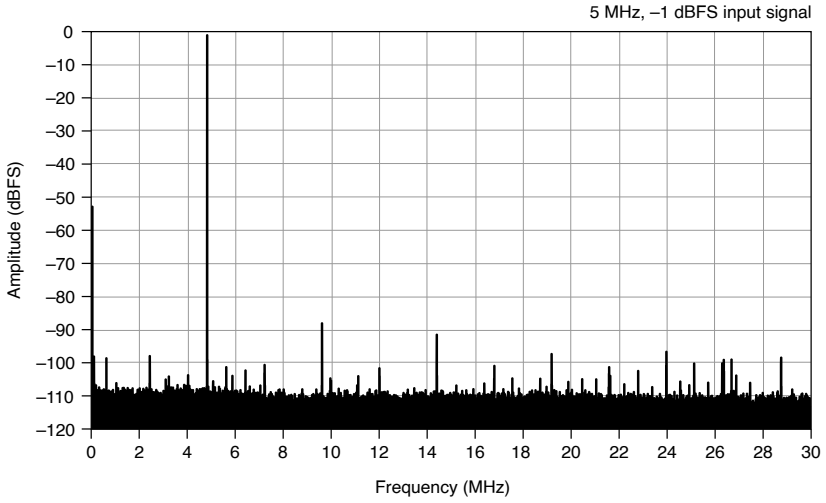
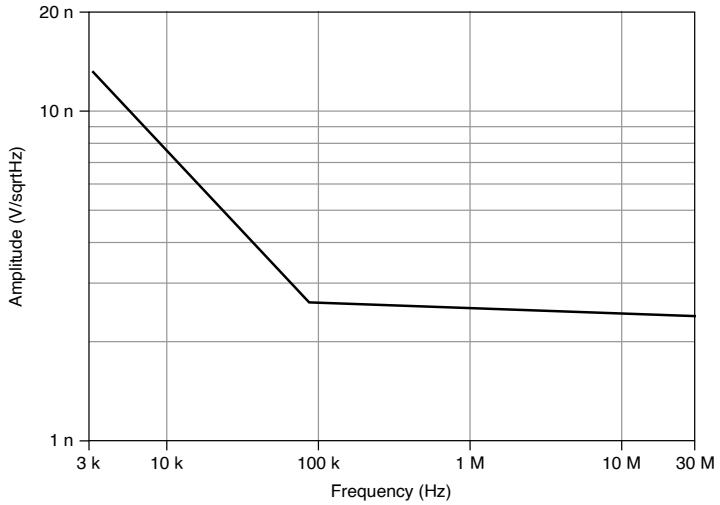


Figure 1. PCI-5105 Spectral Noise Density, 50 Ω, 0.05 V_{pk-pk}, with Anti-alias Filter Enabled, Nominal



50 Ω Noise

Input Range (V_{pk-pk})	Full Bandwidth	24 MHz Filter Enabled
0.05 V	0.08% of FS (40 µV) (≥5 kHz)	0.038% of FS (19 µV) (≥5 kHz)
0.2 V	0.04% of FS (80 µV) (≥5 kHz)	0.028% of FS (56 µV) (≥5 kHz)
1 V	0.03% of FS (300 µV)	0.029% of FS (290 µV)
6 V	0.03% of FS (1.8 mV)	0.028% of FS (1.68 mV)

Table 12. 50 Ω RMS Noise[9]

Skew

Channel-to-channel skew[10]	
24 MHz bandwidth filter disabled	≤500 ps
24 MHz bandwidth filter enabled	≤600 ps

Horizontal

Sample Clock

Sources	
Internal	Onboard clock (internal VCXO)[11]
External	PFI 1
External frequency range	4 MHz to 65 MHz
Exporting[12]	
Destination	PFI 1
Maximum frequency	65 MHz

Onboard Clock (Internal VCXO)

Real-time sample rate range[13]	915.5 S/s to 60 MS/s
Timebase frequency	60 MHz

Timebase accuracy	
Not phase-locked to Reference clock	±25 ppm, warranted
Phase-locked to Reference clock	Equal to the Reference clock accuracy
Sample clock delay range	±1 Sample clock period
Sample clock delay resolution	<10 ps

External Sample Clock

Source	PFI 1 (front panel SMB connector)
Frequency range[14]	4 MHz to 65 MHz[15]
Duty cycle tolerance	45% to 55%

Phase-Locked Loop (PLL) Reference Clock

Sources	PFI 1 (front panel SMB connector) RTSI 7
Frequency range[16]	5 MHz to 20 MHz in 1 MHz increments
Duty cycle tolerance	45% to 55%
Exported Reference clock destination	PFI 1

Triggers

Reference (Stop) Trigger

Supported trigger	Reference (stop) trigger
Trigger types	Edge Window Hysteresis Digital Immediate Software
Trigger sources	CH 0 to CH 7 PFI 1 RTSI <0..6> Software
Time resolution	Sample clock timebase period
Minimum rearm time[17]	
Internal Onboard clock	2.4 µs
External Sample clock	144 × External clock period
Holdoff	From rearm time up to [(2^{32} - 1) × Sample clock timebase period]

Delay	From 0 up to [(2^{32} - 1) - Requested posttrigger samples] × (1/Actual sample rate), in seconds

Analog Trigger

Trigger types	Edge Window Hysteresis
Sources	CH 0 to CH 7 (front panel SMB connectors)
Trigger level range	100% FS
Edge trigger sensitivity	2% FS
Trigger jitter	Sample clock timebase period

Digital Trigger

Trigger type	Digital
Sources	PFI 1 (front panel SMB connector) RTSI <0..6>

Programmable Function Interface

Connector	PFI 1 (front panel SMB connector)

Direction	Bidirectional
Coupling	AC DC

As a Sample Clock or Reference Clock

Input voltage range	
Sine wave	0.65 V_{pk-pk} to 2.8 V_{pk-pk} (0 dBm to 13 dBm)
Square wave	0.2 V_{pk-pk} to 2.8 V_{pk-pk}

Maximum input overload	7 V_{rms} with |Peaks| ≤10 V
Input impedance	50 Ω
Coupling	AC

As an Input (Digital Trigger)

Destinations	Start trigger (acquisition arm) Reference (stop) trigger Arm Reference trigger Advance trigger
Input impedance	150 kΩ, nominal

V_{IH}	2.0 V
V_{IL}	0.8 V
Maximum input overload	-0.5 V, 5.5 V
Maximum frequency	65 MHz

As an Output

Sources	Start trigger (acquisition arm) Reference (stop) trigger End of record Done (end of acquisition) Sample clock timebase Reference clock
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum drive current	±24 mA

Waveform Specifications

Onboard memory size options[18]	16 MB

	128 MB 512 MB
Minimum record length	1 sample
Number of samples[19]	
Pretrigger	Zero up to full record length
Posttrigger	Zero up to full record length
Allocated onboard memory per record[20]	[(Record length in samples × 2 bytes/sample × number of enabled channels) + 480] rounded up to the nearest 128 bytes

Calibration

External Calibration

External calibration calibrates the onboard references used in self-calibration and the external trigger levels. All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for gain, offset, triggering, and timing errors for all input ranges.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[21]	15 minutes

Software

Driver Software

Driver support for this device was first available in NI-SCOPE 3.2.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PCI-5105. NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PCI-5105 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single program.

> **Note** InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE–specific soft front panel instead of InstrumentStudio.

Interactive control of the PCI-5105 was first available via InstrumentStudio in NI-SCOPE 18.1 and via the NI-SCOPE SFP in NI-SCOPE 14.1. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PCI-5105. MAX is included on the driver media.

TClk Specifications

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the **NI-TClk Synchronization Help**, which is located within the **NI High-Speed Digitizers Help**. For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support.

Intermodule SMC Synchronization Using NI-TClk for Identical Modules

Specifications are valid for modules installed in one NI PXI-1042 chassis. These specifications do not apply to PCI modules. Specifications are valid under the following conditions:

- All parameters are set to identical values for each SMC-based module.
- Sample clock set to 60 MS/s.
- All filters are disabled.

> **Note** Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules.

Skew[22]	500 ps
Average skew after manual adjustment[23]	<10 ps

Sample clock adjustment resolution	<10 ps

Power

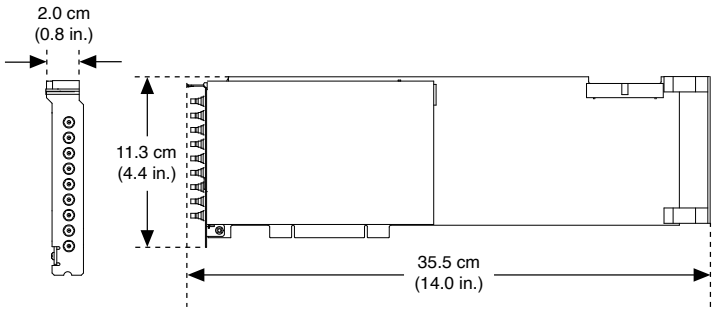
Current draw	
+3.3 V DC	1.7 A
+5 V DC	2 A
+12 V DC	20 mA
-12 V DC	0 A
Total power	15.85 W

Physical

Dimensions and Weight

Dimensions	35.5 cm × 2.0 cm × 11.3 cm (14.0 in. × 0.8 in. × 4.4 in.)
Weight	433 g (15.2 oz)

Figure 1. PCI-5105



Front Panel Connectors

Label	Connector Type	Description
CH 0—CH 7	SMB jack	Analog input connection; digitizes data and triggers acquisitions.
PFI 1		PFI line for trigger input/output, External clock in, Reference clock input/output, and timebase out.

Table 13. PCI-5105 Front Panel Connectors

Environment

Maximum altitude	2,000 m (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

> **Note** For UL and other safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Commitment to the Environment** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

> **EU Customers** At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

> **中国客户** National Instruments 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

[1] AC coupling available on 1 MΩ input only.

[2] Within ±5 °C of self-calibration temperature.

[3] For a 50 kHz signal with amplitude 90% of full-scale input range measured within ±5 °C of self-calibration temperature.

[4] Measured from one channel to another channel, with same range settings on both channels.

[5] AC coupling available on 1 MΩ input only.

[6] -1 dBFS input signal. Includes the second through the fifth harmonics. 24 MHz bandwidth filter enabled.

[7] Verified using a 50 Ω terminator connected to input.

[8] -1 dBFS input signal. Includes the second through the fifth harmonics. 24 MHz bandwidth filter enabled.

[9] Verified using a 50 Ω terminator connected to input.

[10] 10 MHz sine input signal.

[11] Internal Sample clock is locked to the Reference clock or derived from the onboard VCXO.

[12] You cannot export a decimated Sample clock signal.

[13] Divide by **n** decimation used for all rates less than 60 MS/s. For more information about the Sample clock and decimation, refer to the NI High-Speed Digitizers Help.

[14] Divide by **n** decimation available where 1 ≤ **n** ≤ 65,535. For more information about the Sample clock and decimation, refer to the NI High-Speed Digitizers Help.

[15] The PCI-5105, when using NI-SCOPE 3.2, supports a limited frequency range of 8 MHz to 65 MHz.

[16] Default of 10 MHz. The PLL Reference clock frequency must be accurate to ±50 ppm.

[17] Holdoff set to 0. Onboard Sample clock at maximum rate.

[18] Onboard memory is shared between all enabled channels.

[19] Single-record and multirecord acquisitions.

[20] The maximum number of records is 100,000.

[21] Warm-up time begins after the NI-SCOPE driver is loaded. Unless manually disabled, the NI-SCOPE driver automatically loads with the operating system and enables the module.

[22] Caused by clock and analog path delay differences. No manual adjustment performed.

[23] For more information about manual adjustment, refer to the **Synchronization Repeatability Optimization** topic in the **NI-TClk Synchronization Help**.